ABSTRACT

An integrated circuit comprising a processor, a memory that the processor can access, a memory access unit for controlling accesses to the memory, an input for receiving power for the integrated circuit from an external power source, and a power detection unit, the power detection unit being configured to: monitor a quality of power supplied to the input; and in the event the quality of the power drops below a predetermined threshold, disabling a power supply to circuitry for use in writing to the memory, such that the memory access unit's ability to alter data in the memory is disabled prior to address or data values to be written to the memory becoming unreliable due to failing power.